METHODS TO FORM A MEMORY CELL WITH METAL-RICH METAL CHALCOGENIDE

Background of the Invention

Field of the Invention

[0001] The invention generally relates to memory technology. In particular, the invention relates to memory devices with a metal-rich metal chalcogenide, such as silver-rich silver selenide.

Description of the Related Art

[0002] Computers and other digital systems use memory to store programs and data. A common form of memory is random access memory (RAM). Many memory devices, such as dynamic random access memory (DRAM) devices and static random access memory (SRAM) devices are volatile memories. A volatile memory loses its data when power is removed. In addition, certain volatile memories such as DRAM devices require periodic refresh cycles to retain their data even when power is continuously supplied.

[0003] In contrast to the potential loss of data encountered in volatile memory devices, nonvolatile memory devices retain data when power is removed. Examples of nonvolatile memory devices include read only memory (ROM), programmable read only memory (PROM), erasable programmable read only memory (EPROM), electrically erasable programmable read only memory (EEPROM), Flash ROM, and the like.

[0004] One type of memory device is known as a programmable conductor memory cell or a programmable metallization cell (PMC). See U.S. Patent Nos. 5,761,115; 5,896,312; 5,914,893; and 6,084,796 to Kozicki, et al., entitled "Programmable metallization cell structure and method of making same," the disclosures of which are hereby incorporated by reference in their entirety herein. Also see PCT publications WO 00/48196 and WO 02/21542 for additional information. Another term used to describe this cell is a resistance variable material cell. These memory cells can be nonvolatile. A programmable conductor random access memory (PCRAM) includes an array of programmable metallization cells or

resistance variable material cells. Additional applications for a programmable metallization cell include use as a programmable resistance and a programmable capacitance.

[0005] Information can be stored in a resistance variable material cell by forming or by disrupting conductive pathways, which varies the resistance of the cell. In response to an applied electric field, which can be generated by an electric potential applied between electrodes, a conductive pathway grows from an electrode configured as the cathode, i.e., the electrode with the more negative electric potential, to an electrode configured as the anode, i.e., the electrode with the more positive electric potential. Information can be read or retrieved from the cell by sensing the resistance of the cell.

[0006] Conventional processes include techniques that diffuse silver (Ag) through a silver-permeable material, such as a chalcogenide glass. One example of a chalcogenide glass is germanium selenide (Ge_xSe_{1-x}). For example, one conventional process for producing a PMC applies silver (Ag) photodoping to a chalcogenide glass, such as germanium selenide, e.g., Ge_3Se_7. It is relatively difficult to diffuse silver uniformly across a wafer using conventional techniques. For example, in one conventional process, the doping of the silver varies across the wafer by about 5 to 10%, which can reduce production yield.

[0007] Silver-rich silver selenide is relatively difficult to produce using direct deposition techniques. For example, when silver (Ag) is directly deposited on silver selenide ($Ag_{2-\delta}Se$), where $0 \leq \delta \leq 1$, in an attempt to create silver-rich silver selenide ($Ag_{2+x}Se$), the silver (Ag) may agglomerate on the silver selenide and create a rough surface. Similar results may occur when attempting to deposit silver selenide (Ag_2Se) directly on silver (Ag).

[0008] What is needed is a process to enrich a material, including non-transparent materials, with a metal, such as silver (Ag), to fabricate materials such as silver-rich silver selenide ($Ag_{2+x}Se$) or silver-rich silver telluride ($Ag_{2+x}Te$). Such materials can be useful in cell bodies of memory devices.

Summary of the Invention

[0009] The invention relates to the fabrication of a resistance variable material cell or programmable metallization cell (PMC). Advantageously, the processes described herein can form a layer of a metal-rich metal chalcogenide, such as silver-rich silver selenide ($Ag_{2+x}Se$), without the use of photodoping techniques and without direct deposition of the

metal. Further advantageously, the processes can dope a metal, such as silver, into materials that are not transparent. In addition, the processes can form materials such as silver-rich silver selenide ($Ag_{2+x}Se$) with relatively high uniformity and with relatively precise control.

[0010] One process according to an embodiment of the invention forms silver-rich silver selenide ($Ag_{2+x}Se$) for a cell body for a resistance variable material cell. The process includes forming a layer of silver selenide, implanting oxygen to form selenium oxide, and annealing to remove the selenium oxide, thereby forming the silver-rich silver selenide ($Ag_{2+x}Se$). In one embodiment, regions of a wafer are selectively enriched with silver by patterning the oxygen implantation. One embodiment of the process repeatedly performs implanting of oxygen and annealing to increase an amount of silver in the silver-rich silver selenide.

Brief Description of the Drawings

[0011] These and other features of the invention will now be described with reference to the drawings summarized below. These drawings (not to scale) and the associated description are provided to illustrate preferred embodiments of the invention and are not intended to limit the scope of the invention.

[0012] Figure 1 is a flowchart, generally illustrating a process for forming silver-rich silver selenide ($Ag_{2+x}Se$).

[0013] Figure 2A is a cross-sectional view illustrating a resistance variable material cell according to one embodiment of the invention.

[0014] Figure 2B is a cross-sectional view illustrating a resistance variable material cell with a conductive plug according to one embodiment of the invention.

[0015] Figures 3 A-E are cross-sectional views illustrating an array of resistance variable material cells in various stages of construction.

[0016] Figure 4 is a schematic top-down view that illustrates an array of resistance variable material cells in a cross-point configuration.

Detailed Description of Preferred Embodiments

[0017] Although this invention will be described in terms of certain preferred embodiments, other embodiments that are apparent to those of ordinary skill in the art, including embodiments that do not provide all of the benefits and features set forth herein,

are also within the scope of this invention. For example, while illustrated in the context of particular materials, the skilled artisan will appreciate that the methods described herein are applicable to doping a variety of materials with tailored amounts of metal, for a variety of applications. Accordingly, the scope of the invention is defined only by reference to the appended claims.

[0018] One process according to an embodiment of the invention can form silver-rich silver chalcogenide for use in a resistance variable material cell. The silver-rich silver chalcogenide cells include at least one layer of a silver-rich silver chalcogenide and at least one layer of a chalcogenide glass, such as germanium selenide (Ge_xSe_{1-x}). The process can be automated such that it is under computer control. Advantageously, the process is capable of increasing the silver content of materials in a relatively uniform and well-controlled manner. For example, the process can form silver-rich silver selenide ($Ag_{2+x}Se$), silver-rich silver telluride, and the like. The silver-rich regions can be formed in a pattern across a wafer. Cells in an array of cells can be patterned to remove non-enriched regions.

[0019] These silver-rich silver chalcogenide cells can be used to store memory states, programmed resistances, and the like. When an electric potential is applied between the first electrode and the second electrode, a conductive pathway is formed or is disrupted (depending upon the polarity of the potential) in a layer of silver-permeable material, such as germanium selenide (Ge_xSe_{1-x}), thereby varying the resistance of the cell. The formation of the conductive pathway lowers the resistance between the electrodes. The conductive pathway can persist after the removal of the applied electric potential. This property can permit some embodiments of a resistance variable material cell to retain information in a nonvolatile manner.

[0020] While the silver chalcogenide is illustrated primarily in the context of silver selenide, the skilled artisan will appreciate that the principles and advantages described herein are applicable to other silver chalcogenides. For example, other applicable silver chalcogenides can also include silver sulfide and silver telluride.

[0021] Figure 1 is a flowchart, generally illustrating a process for forming silver-rich silver selenide ($Ag_{2+x}Se$) for use in a cell body of a resistance variable material cell. Silver-rich silver selenide ($Ag_{2+x}Se$) includes more silver than stoichiometric silver selenide

(Ag_2Se). In the illustrated process, the process advantageously forms the silver-rich silver selenide ($Ag_{2+x}Se$) without direct deposition of silver (Ag) and without photodoping. Advantageously, a resistance variable material cell can be formed on a variety of substrates and not just semiconductor substrates. For example, a resistance variable material cell can be formed on a plastic substrate. However, the substrate assembly can correspond to a semiconductor, such as a silicon wafer, to facilitate the integration of the cell with electronic devices, such as switches or transistors. The substrate should be electrically insulating or covered with a layer of insulating material to allow a difference in electric potential to be applied between electrodes of a variable resistance material cell.

[0022] The process forms 110 a lower electrode on the substrate assembly. The process can form 110 the lower electrode by forming a conductive film, which can be formed from a variety of materials, such as tungsten (W), tungsten nitride (WN), polysilicon, and others. It will be understood by one of ordinary skill in the art that the lower electrode can also include a barrier layer.

[0023] The process can proceed to form 115 a layer of chalcogenide glass, such as germanium selenide (Ge_xSe_{1-x}), on the lower electrode. The process can include forming the layer of chalcogenide glass below a layer of silver selenide, above the layer of silver selenide, or both. It will thus be understood that in some embodiments of the process, the forming 115 of the layer of chalcogenide glass on the lower electrode is optional. Where the layer of chalcogenide glass is formed 115 on the lower electrode, the layer of chalcogenide glass is preferably between about 50 angstroms (Å) to about 1000 (Å) thick. In one embodiment, the layer of chalcogenide glass is about 150 Å thick. An exemplary chalcogenide glass is Ge_4Se_6.

[0024] The process proceeds to form 120 the layer of silver selenide. It will be understood that the layer of silver selenide can be formed on the lower electrode when the process does not form a layer of chalcogenide glass below the layer of silver selenide. When the process forms the layer of chalcogenide glass on the lower electrode, the layer of silver selenide can be formed on the layer of chalcogenide glass. Although the layer of silver selenide can be formed with stoichiometric silver selenide (Ag_2Se), it will be understood that the silver selenide can also initially be slightly silver-rich or silver-poor, depending on the

deposition process. A variety of techniques can be used to form the layer of silver selenide. Preferably, physical vapor deposition (PVD) techniques, such as evaporative deposition and sputtering, are used to form 120 the layer of silver selenide. In addition, the process can form 120 the layer of silver selenide as a single layer or in multiple layers. Although a variety of techniques are available for forming silver selenide, precise control over the composition is difficult with conventional techniques.

[0025] The process proceeds to implant 130 oxygen. Implanting of oxygen converts at least some of the silver selenide to silver-rich silver selenide ($Ag_{2+x}Se$) and to selenium oxide (SeO_2). A simplified chemical equation (not balanced) is provided in Equation 1.

[0026] $$Ag_2Se + O_2 \rightarrow Ag_{2+x}Se + SeO_2 \quad \text{(Eq. 1)}$$

[0027] Ion implantation techniques are preferably used to implant the oxygen into the layer of silver selenide. Advantageously, ion implantation is a relatively well-controlled process, which correspondingly permits the amount of silver richness, x, in the silver-rich silver selenide ($Ag_{2+x}Se$) to be relatively well controlled. For example, ion implantation techniques can implant oxygen with less than 1% variation across a layer of silver selenide on the surface of a wafer. By contrast, a variation in uniformity of around 5 to 10 percent across the surface of a wafer can be expected from techniques that directly deposit silver or photodope silver.

[0028] Preferably, oxygen is implanted at a relatively high dosage. The high dosage permits the amount of silver richness, x, to be correspondingly high. Preferably, x is in a range of about 0 to about 10%. More preferably, x is in a range of about 1% to about 3%. Preferably, the oxygen is implanted to a relatively shallow depth that is relatively close to the surface. In one embodiment, the oxygen implanter tool is configured to implant oxygen to a depth or range of about 100 (Å) with a setting of about 1 to about 3 kilo-electron volts (keV). In addition, implanting 130 of oxygen and annealing 140 of the substrate assembly can be repeated as described later in connection with an optional decision block 150.

[0029] Implanting 130 of oxygen can be selectively applied to the layer of silver selenide. A pattern mask, such as a mask of photoresist, can be formed over the layer of

silver selenide to allow the ion implantation to implant oxygen to selected areas. The presence of the pattern mask blocks implantation of oxygen from selected areas. The pattern mask includes open windows that permit implantation of oxygen in other areas. In another embodiment, implanting 130 of oxygen is applied to the layer of silver selenide without patterning.

[0030] The process proceeds to anneal 140 the substrate assembly. Annealing 140 removes the selenium oxide from the layer. Where implanting of oxygen has been carried out in a patterned manner, regions of silver selenide (Ag_2Se) and silver-rich/silver selenide ($Ag_{2+x}Se$) are left after annealing. Prior to annealing 140 the substrate assembly, the pattern mask, if present, should be removed.

[0031] Annealing 140 includes heating the substrate assembly in a chamber, which is maintained at a relatively low pressure. In one embodiment, the substrate assembly is heated such that a vapor pressure of selenium oxide (or more generally, the oxide of the element to be removed) is greater than the pressure maintained in an annealing chamber. Annealing 140 can be performed at a broad range of pressures and temperatures. Annealing 140 can be performed for a predetermined time using data collected from experimental results. Endpoint detection techniques, such as optical emission spectroscopy techniques, can also be used to determine when to stop annealing. In one embodiment, annealing 140 is performed at a temperature between about 50 degrees centigrade (C) to about 130 degrees C for a time period of about 30 minutes to about 3 hours. Preferably, annealing is performed at a temperature of about 90 degrees C.

[0032] The process proceeds to an optional decision block 150, where the process determines whether to repeat implanting 130 and annealing 140. Implanting 130 and annealing 140 can be repeated multiple times to increase the amount of silver richness, i.e., the value of x, in silver-rich silver selenide ($Ag_{2+x}Se$). The number of times that implanting 130 and annealing 140 is repeated can be predetermined. A counter, which can be implemented in a computer memory, can track the number of iterations of implanting 130 and annealing 140. If implanting 130 and annealing 140 are to be repeated, the process returns from the optional decision block 150 to implanting 130. Otherwise, the process

proceeds to pattern 160 cells. When implanting 130 is repeated, the process can implant to the same depth or to different depths.

[0033] The process can pattern 160 cells in accordance with a variety of techniques. Patterning techniques that can be used include reactive ion etch (RIE) and ion beam etching (IBE) techniques. In one embodiment, a potassium iodide / iodide (KI/I_2) solution is used with a pattern mask to selectively etch and thereby pattern cells. It will be understood by one of ordinary skill in the art that patterning 160 of cells may require additional steps, such as mask patterning and etching in conjunction with the mask.

[0034] The process can then form 165 a layer of chalcogenide glass on the patterned layer of silver selenide. As described earlier, the process can form the layer of chalcogenide glass below the layer of silver selenide, above the layer of silver selenide, or both. Thus, it will be understood that in some embodiments of the process, the process does not form the layer of chalcogenide glass on the layer of silver selenide.

[0035] The process then forms 170 an upper electrode. The upper electrode can be formed from a variety of materials, such as silver (Ag), titanium (Ti), tungsten (W), tungsten nitride (WN), and the like. When the process forms 165 the layer of chalcogenide glass on the patterned layer of silver selenide, the process can form 170 the upper electrode on the layer of chalcogenide glass. When the process does not form 165 the layer of chalcogenide glass, the process can form 170 the upper electrode on the patterned layer of silver selenide. It will be understood by one of ordinary skill in the art that the upper electrode can also include barrier layers preferably formed from the same metal that dopes the film.

[0036] In another embodiment of the process, the process optionally forms a layer of insulating material between the lower electrode and the upper electrode. One embodiment of a resistance variable material cell or PCRAM cell with such an insulating layer is described in greater detail later in connection with Figure 2B. The insulating layer can be formed on the lower electrode, or the insulating layer can be formed between the silver-rich silver selenide ($Ag_{2+x}Se$) layer and the upper electrode. Advantageously, the insulating layer can prevent the unintended shorting of the lower and upper electrodes. The insulating layer can be formed from a variety of dielectrics including, for example, silicon nitride (Si_3N_4).

The insulating layer includes vias, which can be filled with plugs of conductive material to provide electrical continuity between the lower electrode and the silver-rich silver selenide ($Ag_{2+x}Se$) layer or between the upper electrode and the silver-rich silver selenide ($Ag_{2+x}Se$) layer. An example of a suitable material for such a plug is tungsten (W).

[0037] Figure 2A is a cross-sectional view illustrating a resistance variable material cell 200 according to one embodiment of the invention. The resistance variable material cell 200 can be fabricated on top of a variety of structures including semiconductors and insulators. The resistance variable material cell 200 includes a lower electrode 202. The lower electrode 202 can be formed from a variety of materials, such as tungsten (W), tungsten nitride (WN), and polysilicon.

[0038] A layer of silver-rich silver selenide ($Ag_{2+x}Se$) 206 forms an active layer of a body of the resistance variable material cell 200. The layer of silver-rich silver selenide ($Ag_{2+x}Se$) 206 is disposed between the lower electrode 202 and an upper electrode 210. The illustrated resistance variable material cell 200 also includes a layer of chalcogenide glass, which can be disposed on either side of the layer of silver-rich silver selenide ($Ag_{2+x}Se$) 206. For example, the layer of chalcogenide glass can be disposed between the layer of silver-rich silver selenide ($Ag_{2+x}Se$) 206 and the lower electrode 202 as shown by a lower layer of chalcogenide glass 204. The layer of chalcogenide glass can alternatively be disposed between layer of silver-rich silver selenide ($Ag_{2+x}Se$) 206 and the upper electrode 210 as shown by an upper layer of chalcogenide glass 207. It will be understood that the chalcogenide glass can correspond to a variety of chalcogenide glasses and can include, for example, germanium selenide (Ge_xSe_{1-x}). Preferably, the layer of silver rich silver selenide ($Ag_{2+x}Se$) 206 is between about 100 Å and about 1000 Å thick. More preferably, the layer of silver rich silver selenide ($Ag_{2+x}Se$) 206 is between about 300 Å and about 470 Å thick. The upper electrode 210 can be formed from a variety of materials, such as silver (Ag), titanium (Ti), tungsten (W), tungsten nitride (WN), and the like.

[0039] In response to a difference in electric potential applied between the lower electrode and the upper electrode, a conductive pathway is formed or is disrupted in the resistance variable material cell 200. The conductive pathway (or lack thereof) can persist

after the removal of the applied electric potential. This property can permit a resistance variable material cell to retain information in a nonvolatile manner.

[0040] An insulator 208 insulates the body of the resistance variable material cell 200 from other memory cells and also prevents the undesired diffusion of active material. The insulator 208 can be formed from a variety of materials such as silicon nitride (Si_3N_4). Of course, the insulator 208 can be formed in multiple steps and can include multiple structures.

[0041] Figure 2B is a cross-sectional view illustrating a resistance variable material cell 250 with a conductive plug according to one embodiment of the invention. The illustrated resistance variable material cell 250 includes a plug 214 of conductive material, such as tungsten (W) formed in an opening or via defined in the insulator 208. The plug 214 is disposed between the lower electrode 202 and the upper electrode 210. Advantageously, the addition of the plug 214 can help to prevent the inadvertent or unintended shorting of the lower electrode 202 and the upper electrode 210.

[0042] In the illustrated embodiment of the resistance variable material cell 250, a lower layer of chalcogenide glass 205 is disposed between the plug 214 and the layer of silver-rich silver selenide ($Ag_{2+x}Se$) 206, and an upper layer of chalcogenide glass 207 is disposed between the layer of silver-rich silver selenide ($Ag_{2+x}Se$) 206 and the upper electrode 210. It will be understood that the resistance variable material cell 250 can include those embodiments with only one of the lower layer of chalcogenide glass 205 or the upper layer of chalcogenide glass 207, or embodiments with both as illustrated in Figure 2B.

[0043] In the illustrated embodiment of the resistance variable material cell 250, the plug 214 is disposed between the layer of silver-rich silver selenide ($Ag_{2+x}Se$) 206 and the lower electrode 202. It will be understood by the skilled practitioner that the relative location of the plug 214 and the layer of silver-rich silver selenide ($Ag_{2+x}Se$) 206 can be interchanged, such that the plug 214 can be disposed between the layer of silver-rich silver selenide ($Ag_{2+x}Se$) 206 and the upper electrode 210. It will also be understood that a layer of silver-permeable material, such as a layer of germanium selenide, can also be disposed between the layer of silver-rich silver selenide ($Ag_{2+x}Se$) 206 and the lower electrode 202 or the upper electrode 210.

[0044] The plug 214 should be formed from a conductive material, such as tungsten (W). The illustrated plug 214 provides electrical continuity between the lower electrode 202 and the layer of silver-rich silver selenide ($Ag_{2+x}Se$) 206 or between the lower electrode 202 and the lower layer of chalcogenide glass 205, where present. Preferably, the plug 214 is formed such that the plug 214 is relatively level with the insulator 208 in which an opening or via for the plug 214 is formed.

[0045] The cells of resistance variable materials are preferably arranged in an array of cells. The array advantageously permits a relatively large number of cells, and thereby a relatively large memory space, to be fabricated contemporaneously. Figures 3 A-E are cross-sectional views illustrating an array of resistance variable material cells in various stages of construction. It will be understood by one of ordinary skill in the art that the number of cells in an array can vary in a very broad range. In Figures 3 A-E, three cells are shown for the purposes of illustration.

[0046] Figure 3A illustrates a portion of a substrate assembly with a substrate 302, a first lower electrode 304, a second lower electrode 306, and a third lower electrode 308. The substrate can correspond to a variety of substrates, such as an insulating substrate, a semiconductor substrate, or an insulating layer on a semiconductor substrate. Again, for the purposes of illustration, the memory cells will be described in the context of silver selenide as the metal-doped chalcogenide.

[0047] A layer of silver selenide 310 is formed above the substrate 302, the first lower electrode 304, the second lower electrode 306, and the third lower electrode 308. The layer of silver selenide 310 can be formed from stoichiometric silver selenide (Ag_2Se) or from slightly silver-rich or silver-poor silver selenide.

[0048] Figure 3B illustrates the portion of the substrate assembly with a patterned mask. The patterned mask is formed on top of the layer of silver selenide 310 and is used to permit the selective implantation of oxygen. It will be understood that the layer of silver selenide 310 can be implanted with oxygen without a patterned mask. The illustrated patterned mask includes a first portion of photoresist 312 and a second portion of photoresist 314. In one embodiment, the patterned mask is formed from a layer of photoresist material that is patterned using photolithography. In another embodiment, the patterned mask is form

from a hard mask, such as a mask of silicon nitride. Openings 316 are defined in the pattern mask to selectively provide access to the layer of silver selenide 310 such that oxygen can correspondingly be selectively implanted in the layer of silver selenide 310.

[0049] As illustrated in Figure 3B, a first region 318, a second region 320, and a third region 322 are implanted with oxygen. The oxygen implanter tool can be configured to implant oxygen to a variety of depths. In one embodiment, the depth or range of implantation corresponds to approximately 100 (Å).

[0050] In Figure 3C, the pattern mask is removed, and the substrate assembly is annealed. Annealing removes selenium oxide from the implanted regions of the layer of silver selenide illustrated by the first region 318, the second region 320 and the third region 322, thereby leaving silver-rich regions in the layer of silver selenide. These silver-rich regions are illustrated by a first silver rich-region 328, a second silver-rich region 330, and a third silver-rich region 332. As described earlier in connection with Figure 1, patterning, implanting, and annealing of the silver selenide layer can be repeated multiple times to increase the amount of silver-richness in the silver selenide layer.

[0051] Figure 3D illustrates the first silver-rich region 328, the second silver-rich region 330, and the third silver-rich region 332 that have been patterned into cells from the layer of silver selenide. A variety of techniques can be used to pattern cells including, for example, wet etching, reactive ion etching (RIE) and ion beam etching (IBE) techniques. It will be understood by one of ordinary skill in the art that such patterning techniques can also include additional mask patterning steps.

[0052] In addition, it will be understood that in-between patterning of cells and forming of upper electrodes, a layer of an insulator can be formed to fill the space between the cells. The layer of insulator can be made from a variety of materials, such as silicon nitride or polyimide. A chemical-mechanical polish (CMP) can smooth out the top of the layer of the insulator. A portion of the insulator can also be formed between the cell and the upper electrode, and the vias and plugs can be landed on the layer of silver-rich silver selenide to provide electrical continuity to the upper electrode.

[0053] After patterning of the cells, upper electrodes are formed on top of the cells patterned from the silver rich-regions. For example, Figure 3E illustrates an upper

electrode 334 formed above cells patterned from the first silver-rich region 328, the second silver-rich region 330, and the third silver-rich region 332.

[0054] Figure 4 is a schematic top-down view that illustrates an array of resistance variable material cells in a cross-point configuration. It will be understood that a resistance variable material cell can also be isolated and coupled to transistors for read and write operations. The portion of the array shown in Figure 4 includes 9 resistance variable material cells, but it will be understood by one of ordinary skill in the art that the number of cells in an array can vary in a very broad range. The array includes lower electrodes, as illustrated by a first lower electrode 402, a second lower electrode 404, and a third lower electrode 406. The array also includes upper electrodes, as illustrated by a first upper electrode 408, a second upper electrode 410, and a third upper electrode 412. In the illustrated cross-point configuration, the lower electrodes and the upper electrodes are arranged in an approximately orthogonal manner, but it will be understood that other configurations are possible.

[0055] Memory cells lie between the lower electrodes and the upper electrodes approximately where the electrodes cross. For example, a first resistance variable material cell 414 is disposed between the first lower electrode 402 and the first upper electrode 408. The contents of the first resistance variable material cell 414 can be accessed (for reading or writing) by activating the first lower electrode 402 and the first upper electrode 408. Information can be stored in a cell by forming or by disrupting conductive pathways, which varies the resistance of the cell. When an electric potential is applied between the upper electrode and the lower electrode, an electric field is generated in the layer of resistance variable material. In response to the electric field, a conductive pathway grows from the electrode configured as the cathode, i.e., the electrode with the more negative electric potential, to the electrode configured as the anode, i.e., the electrode with the more positive electric potential. Information can be read or retrieved from the cell by sensing the resistance of the cell.

[0056] Various embodiments of the invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting.

Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined in the appended claims.